WE CLAIM:

1. A computing system comprising:

a processor having a data/control bus interface;

a data/control bus implementing one or more device communication channels;

a data memory coupled to the processor;

a mass storage device having an interface for communicating mass storage transactions; and

a controller having a memory interface coupled to the data memory and a mass storage interface coupled to the mass storage device's interface and operable to conduct mass storage transactions between the data memory and the mass storage device.

2. The computing system of claim 1 wherein the data memory is coupled to the processor by a memory bus operating independent of the data/control bus.

3. The computing system of claim 2 wherein the controller comprises a memory access controller coupled to the processor, the data memory, and the mass storage device and operable to arbitrate accesses to the data memory between the mass storage and the processor.

4. The computing system of claim 2 wherein the controller comprises a direct memory access controller coupled to the data/control bus, wherein the mass storage interface comprises a logical connection formed using one of the device communication channels.

5. The computing system of claim 1 wherein the data memory is coupled to the data/control bus.

6. The computing system of claim 5 wherein the controller comprises a direct memory access controller coupled to the data/control bus and the memory interface

comprises a logical connection formed using one of the device communication channels

7. The computing system of claim 1 further comprising storage controller processes and application behavior processes implemented using the processor.

8. The computing system of claim 7 wherein the storage controller processes map storage requests generated by the application behavior processes expressed in logical geometry terms into storage requests expressed in physical geometry terms.

9. The computing system of claim 1 wherein the data memory includes logic that map storage requests generated by the processor expressed in logical geometry terms into storage requests expressed in physical geometry terms.

10. The computing system of claim 1 wherein the processor implements data structures storing physical geometry information about the mass storage device.

11. The computing system of claim 1 wherein the data/control bus comprises at least one direct memory access (DMA) channel.

12. The computing system of claim 1 wherein the controller is integrated with the processor on a single integrated circuit chip.

13. The computing system of claim 1 wherein the mass storage device's interface comprises a peripheral component interconnect (PCI) standard-compliant interface.

14. The computing system of claim 1 wherein the mass storage device's interface comprises a small computer systems interface (SCSI) standard-compliant interface.

15. The computing system of claim 1 wherein the mass storage device's interface comprises a universal serial bus (USB) standard-compliant interface.

16. The computing system of claim 1 wherein the mass storage device's interface comprises an IEEE 1394 standard-compliant interface.

17. The computing system of claim 1 wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands;

a servo controller coupled to receive requests transferred from the data memory by the controller and generate the commands to the actuator mechanism.

18. The computing system of claim 17 wherein the mass storage device's interface is implemented by the servo controller and implements a physical interface to the data/control bus and a physical interface to the head and actuator mechanism.

19. The computing device of claim 1 wherein the computing device comprises a set-top box including processes for implementing audio/video behaviors in the processor.

20. The computing device of claim 1 wherein the computing device comprises a network appliance having a network controller coupled to the data/control bus.

21. The computing device of claim 1 wherein the mass storage device comprises an optical storage device.

22. The computing device of claim 1 wherein the mass storage device comprises a magneto-optical storage device.

23. A mass storage device comprising:

a surface for storing data;

a head for accessing the stored data;

a storage controller executing requests for positioning the head at specified locations with respect to the surface and accessing data at the specified location, wherein the storage controller includes processing resources for executing non-storage related program code.

24. The mass storage device of claim 23 further comprising a rotating disk having the surface for storing data formed thereon.

25. The mass storage device of claim 24 further comprising:

an actuator coupled to the head for moving the head to specified locations over the disk's surface in response to commands generated by the storage controller.

26. The mass storage device of claim 25 wherein the storage controller comprises:

27. The mass storage device of claim 23 further comprising a tape having the surface for storing data formed thereon.

28. A computing system architecture comprising:

a data processor executing both storage control processes and general-purpose processes;

a data memory coupled to the data processor to implement memory transactions generated by the data processor; and

a mass storage device having an interface communicating with the storage control processes through the data memory.

29. A method for operating a computing system comprising:

providing a data processing system for executing instructions to manipulate data according to the executed instruction;

coupling stored instructions to the data processor;

storing in memory accessible to the processor parameters describing a physical geometry of a mass storage system; and

executing both storage-related instructions and application related instructions in the same processor.

30. The method of claim 29 wherein the storage-related instructions include instructions using the physical geometry parameters.

31. The method of claim 29 wherein the storage related instructions include instructions implementing read channel functionality.